REMARKS

The Office Action dated 13 April 2005 has been reviewed, and the comments of the Patent Office considered. Claims 1 and 3 have been amended, claim 2 was previously presented, claims 4-9 remain as originally filed, and claims 10-20 have been canceled without prejudice or disclaimer. Thus, claims 1-9 are respectfully submitted for reconsideration by the Examiner.

The indication that claim 3-9 contain allowable subject matter is greatly appreciated. In accordance with the Examiner's helpful suggestion, claim 3 has been rewritten in independent form. Thus, it is respectfully submitted that the objections should be withdrawn and that claim 3, as well as claims 4-9 that depend directly or indirectly from claim 3, should be allowed.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent Application Publication No. 2004/0093457 to Heap in view of U.S. Patent No. 5,668,974 to Grassi et al. ("Grassi"). This rejection is respectfully traversed in view of the above amendment to claim 1 and the following comments.

Applicant's claim 1 recites a memory interleave controller that, *inter alia*, stores a code in a nonvolatile ferroelectric memory in order to differently control memory interleave operations depending on an access latency time and a restore latency time of address set within a range of memory interleave corresponding to lower address bits among row address bits, and changes an address path of a single chip FeRAM array.

The Office Action appears to allege that the features recited in Applicant's claims 1 and 2 correspond to those of Heap as set out in Table 1.

Table 1

Applicant's Device	Heap
Single chip FeRAM array 50	Memory array 903
Memory interleave controller 40	Memory controller 901
Bus 60	Data bus 907

However, Heap's Figure 11A appears to show a memory controller 901 that includes logic circuits 1101 and 1102 and an address mapper 1001, and that determines a bank address depending on the result of ANDing, and then forwards a mapped address and control information

to the memory bank 903. That is, Heap's memory controller 901 does not differently control interleave operations depending on an access latency time and a restore latency time of address set up in a nonvolatile ferroelectric memory, as recited in Applicant's claim 1.

In particular, Applicant's interleave controller 40 programs a code of interleave operation in a nonvolatile ferroelectric memory in order to differently control an access time of a FeRAM array, based at least in part on difference of latency time required according to kinds of address. Thus, Heap fails to teach or suggest at least Applicant's nonvolatile ferroelectric memory.

For at least the reasons discussed above, it is respectfully submitted that Heap fails to teach or suggest an memory interleave controller as recited in Applicant's claims 1 and 2. Moreover, it is respectfully submitted that Grassi fails to overcome the deficiencies of Heap.

The Office Action appears to allege that the features recited in Applicant's claims 1 and 2 correspond to those of Grassi as set out in Table 2.

Table 2

Applicant's Device	Heap
Single chip FeRAM array 50	Memory 103
Single banks 51 and 52	Module pair M1A and M1B
Memory interleave controller 40	Memory configuration unit 14
Nonvolatile interleave program register 41	Registers 54~65
Interleave controller 42	Decoder 17

However, Grassi shows a decoder 17, which is included in the memory configuration unit 14, for changing an address path. That is to say, Grassi appears to show selecting a module based on a selection signal SEL that is outputted from the decoder 17, but does not differently control memory interleave operations depending on an access latency time and a restore latency time of address, as is recited in Applicant's claims 1 and 2. In fact, it is respectfully submitted that Grassi shows an entirely different technique to control a memory interleave operation.

The Office Action also alleges that Grassi's registers 54~65 correspond to Applicant's nonvolatile interleave program register 41. However, in contrast to Grassi, Applicant's

interleave controller 40 independently controls memory interleave operations depending on the kinds of address, thereby reducing a row access latency time and a restore latency time. Moreover, Applicant's device stores in a nonvolatile type memory information of interleave operations so that configure data is not lost, even when power is turned off.

For at least the above reasons, it is respectfully submitted that Applicant's claims 1 and 2 recite combinations of features that are neither taught nor suggested by Heap and/or Grassi, whether considered individually or in combination. Therefore, it is respectfully submitted that the rejections under 35 U.S.C. § 103(a) should be withdrawn and that Applicant's claims 1 and 2 also be allowed.

CONCLUSION

In view of the above remarks, Applicant respectfully requests that all objections and rejections be withdrawn and that a notice of allowance be forthcoming. The Examiner is invited to contact the undersigned for any reason related to the advancement of this case.

The Commissioner is hereby authorized to charge any additional fees due under 37 C.F.R. § 1.17 or credit any overpayment to Deposit Account 08-1641.

Respectfully submitted,

Date: 13 July 2005

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